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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,683	04/20/2001	Robert L. Shuler JR.	MSC-22953-3	5289

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NASA JOHNSON SPACE CENTER
MAIL CODE HA
2101 NASA RD 1
HOUSTON, TX 77058

EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,683	SHULER, ROBERT L.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,10-16 and 22-37* is/are pending in the application.

4a) Of the above claim(s) *14-16 and 22-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,10-13 and 30-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response To Amendment

1. This office action is responsive to the amendment filed on 9/23/04.

2. The objection to the drawings in the last office action has been overcome based on applicant's drawings filed on 6/23/04.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: "changing a width of the first FET" in claim 32, and "making the first channel wider" in claim 33.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 11-13 and 30-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 11, "further comprising a plurality of logic gates ... fan out" is indefinite because it is not know which elements are for the "plurality of logic gates" in the elected embodiments. Clarification and/or appropriate correction is requested.

Claims 12 and 13 are indefinite because of the "plurality of logic gates" as in claim11, and also because they include the indefiniteness of claim 11.

With respect to claim 30, the recitation "providing one or more logic gates for said circuit with a feedback path from an output of a respective one or more logic gates to an input thereof" is indefinite because it is misdescriptive. It is seen in the elected embodiments (Figures 6, 11A, 11B, and 13) that there is only one logic gate (e.g., 612, Figure 6) for the circuit with a feedback path from the output of the logic gate to the input of the logic gate. Thus, it is not understood which elements are for the more than one logic gates (i.e., the second one, the third one, etc). Also in claim 30, "the one or more logic circuits" on lines 8, 11, 16 and 22 lacks antecedent basis and it appears that "the one or more logic circuits" needs to be changed to --the one or more logic elements--. Further, "a subsequent logic element" is indefinite because it is unclear whether "a subsequence logic element" is the same as the "respective one of the one or more logic elements or of the one or more logic gates", or whether it is an additional logic element. Also, "the subsequence logic device" on line 18 lacks antecedent basis.

Claims 31-37 are indefinite because they include the indefinite problems of claims 31 and/or 32 as discussed above.

Also in claim 31, "said providing step" is indefinite because it is unclear which one of the "providing step" it is referred to since there a multiple of providing recited earlier in the independent claim 30 (e.g., lines 5, 8, 13 and 20 in claim 30). Further, the recitation "adjusting the characteristics of the first channel of the first FET" of the one or more logic gates in claim 31 appears to be misdescriptive because the disclosure only discloses adjusting the channel of the FETs of the embedded delay (i.e., the FETs of the logic elements in the claims, see pages 9 and 10 of the instant specification), and not for the FETs of the logic gates. Clarification and/or appropriate correction is required.

Claims 32-36 are also indefinite because they include the indefiniteness of claim 31.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Bansal (USP 5,504,703).

With respect to claim 8, Figure 3 of the Bansal reference discloses a latch circuit, which includes: a logic gate (T1, T2) having an input (node 4) and an output (node 1); and a feedback path (path goes from node 1 to node 4) from the output (node 1) to the input (node 4) of the logic gate, wherein the feedback path includes two or more delay elements (INV1, INV2, INV3, INV4); wherein the logic gate and the two or mode delay elements each comprising an input to output pulse response (input-to-output signal) operable for delaying a propagation time of a pulse propagating therethrough and for selectively reducing a pulse width therefore (due to the delay propagate therethrough and the delay of the rise time and fall time of the logic gate/element that the signal is propagated therethrough); and the logic gate and the two or more logic elements being operable for reducing in size an instance of a potentially SEU producing glitch introduce at the input of the logic gate before the potential SEU producing glitch propagates through the feedback path to the input of the logic gate (i.e., configured to absorb a glitch at the input of the logic gate before it propagates through the feedback path to the input of the logic gate, Col. 3, lines 28-36 and 52-64), the input to output pulse response of the logic gate and the two or more

logic elements being substantially similar in that the resulting amount of pulse propagation delay and amount of reducing of the pulse width of the potential SEU producing glitch is spread substantially evenly among the logic gate and the two or more logic elements (because every logic element must have a delay therein. Further, because every element in the latch is an inverter, and because reference does not specifically state the delay of each inverters in the latch is different, so the delay of each inverter in the latch is the same, so that the delay being spread evenly among the logic gate and the inverters in the feedback path).

Note with claim 10, as discussed in claim 9 above, because every element in the latch is an inverter, and because reference does not specifically state the rise time and fall time of each inverters in the latch is different, so the rise time and fall time of each inverter in the latch is the same.

Insofar as understood in claims 30 and 37, the circuit in Figure 3 of Bansal as discussed above meets the limitations of claim 10 as the one more logic gates (T1-T2, T3-T4), and the one or more logic elements (INV1-INV4). Note that, regarding to the limitation of pulse width L1 and pulse width L2, these limitations are met in the operation of the circuitry because each logic element in the circuit must have a delay, and if a glitch having a pulse width that is too small (i.e., less than a predetermined threshold pulse width, say L1) then the glitch cannot pass through a respective of the one or more logic gates and/or a respective of the one or more logic elements because such pulse width of the glitch is too small to trigger a logic device/circuit; and if the glitch has a pulse width greater than the predetermined threshold pulse width (L1) and less than a certain pulse width L2 (i.e., the pulse width is large enough to be affected by the delay of the logic device/circuit) then the glitch will pass through the respective of the one or more logic

elements and of the one or more logic gates because the pulse width of the glitch is long enough to trigger the logic device/circuit and the output pulse width of the glitch then has a reduce pulse width (due to the delay rise time and fall time of the respective logic device/circuit). Note that the delay spread evenly is also met as discussed in claim 1 above. Also, the circuit in Figure 3 is a latch circuit.

Response to Arguments

8. Applicant's arguments filed 9/23/04 have been fully considered but they are not persuasive.

Applicant argues that Bansal does not specifically say whether or not the delay is different (or spread evenly) as between the logic gate and the inverters in the feedback path. However, this argument is not persuasive because every element in the latch is an inverter, and because reference does not specifically state the delay of each inverter in the latch is different, so the delay of each inverter in the latch is the same. Note that, in the art, if the two inverters having different size or delay, then the reference will be indicated specifically; and if the reference is silent about the size or delay, then it is assume that the size and the delay of the two inverters are the same.

Conclusion

9. Note with claims 11-13 and 31- 36, in view of the significant indefiniteness problems noted above, no prior art can be applied against these claims at this time. This is <u>not</u> an indication of allowability to these claims.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 10, 2004

Long Nguyen
Primary Examiner
Art Unit: 2816